[Document] Abstract

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[Problem]

The present invention is intended to provide an image data reducing device, a micro computer, and an electronic apparatus that can reduce image data without causing the increase in circuit scale and over spec.

[Means to Solve the Problem]

An image data reducing device 100 comprises a reduced image data generating circuit 180 to which each component of YUV is input in series and that outputs YUV image data after reduced, and an output control signal generating circuit 190 that generates an output control signal 122 for controlling whether each component of YUV is output or not. The reduced image data generating circuit 180 includes a switching circuit that controls the presence of output for each component of image data input in series based on the output control signal 122. The output control signal generating circuit 190 includes a counting circuit 130 that counts input of Y component and resets the counted value when the counted value reaches the reciprocal number of reduction ratio, and a decimation pattern information storing unit 140 that stores decimation pattern information set in correlation with the counted value of the Y component. The output control signal generating circuit 190 generates an output control signal based on the counted value of the Y component and the decimation pattern information.

[SELECTED FIGURE]
FIG. 2

[CLAIMS]
[Claim 1]

An image data reducing device for image data composed of a plurality of components, the image data having data corresponding one-to-one to each pixel with respect to a given component among the plurality of components, and having data common to a plurality of pixels with respect to the other components, the image data reducing device, comprising:

a reduced image data generating circuit receiving image data that is input so that data of each component has a series relationship with each other, and generating image data after reduced so as to output the image data after reduced; and

an output control signal generating circuit generating an output control signal for controlling whether each component of input image data is output or not based on a decimation pattern of input component that is determined depending on a format of input image data and reduction ratio, wherein the reduced image data generating circuit comprises a switching circuit controlling the presence of output for each component of image data input in series based on the output control signal.

[Claim 2]

The image data reducing device according to Claim 1, wherein:

the output control signal generating circuit comprises:

a counting circuit counting input of the given component, and resetting counted value in the case where the counted value reaches the reciprocal number of the reduction ratio so as to restart counting, based on information about the format of image data and information about the reduction ratio; and

a decimation pattern information storing unit storing decimation pattern information set in correlation with the counted value of the given component, wherein the output control signal is generated based on the counted value of the given component and the decimation pattern information.

[Claim 3]

An image data reducing device reducing YUV image data, comprising:

a reduced image data generating circuit receiving image data that is input so that data of each component of YUV has a series relationship with each other, and generating YUV image data after reduced so as to output the YUV image data after reduced; and

an output control signal generating circuit generating an output control signal for controlling whether each component of YUV of input image data is output or not based on a decimation pattern of input

component that is determined depending on a format of input YUV image data and reduction ratio, wherein:

the reduced image data generating circuit comprises a switching circuit controlling the presence of output for each component of image data input in series based on the output control signal;

the output control signal generating circuit comprises:

a counting circuit counting input of Y component, and resetting counted value in the case where the counted value reaches the reciprocal number of the reduction ratio so as to restart counting, based on information about the format of image data and information about the reduction ratio; and

a decimation pattern information storing unit storing decimation pattern information set in correlation with the counted value of the Y component; and

the output control signal is generated based on the counted value of the Y component and the decimation pattern information.

[Claim 4]

The image data reducing device according to any of Claims 1 through 3, wherein:

the reduced image data generating circuit comprises a common data storing unit retaining the other components or UV component that is input and has data common to a plurality of pixels, the reduced image data generating circuit generating reduced image data by using data stored in the common data storing unit based on the output control signal; and

the output control signal generating circuit determines whether reduced image data is generated by using data stored in the common data storing unit or not, based on the counted value of the Y component and the decimation pattern information, the output control signal generating circuit generating the output control signal directing to generate reduced image data by using data stored in the common data storing unit in the case where generating of reduced image data by using data stored in the common data storing unit is determined.

[Claim 5]

The image data reducing device according to any of Claims 1

through 4, wherein:

input data is received as parallel data with bandwidth equal to a bit number of each component; and

the reduced image data generating circuit controls the presence of output for each bit of the parallel data base on the output control signal.

[Claim 6]

The image data reducing device according to any of Claims 1 through 5, wherein:

a reduction ratio setting register setting reduction ratio information is included; and

reduction ratio is determined based on the reduction ratio information set in the reduction ratio setting register.

[Claim 7]

The image data reducing device according to any of Claims 1 through 6, wherein:

a format information setting register setting format information of input image data is included; and

a format of input image data is determined based on the format information set in the format information setting register.

[Claim 8]

A micro computer comprising the image data reducing device according to any of Claims 1 through 7.

[Claim 9]

An electronic apparatus, comprising:

the micro computer according to Claim 7;

input means for data to be processed by the micro computer; and

LCD output means for outputting data that has been processed by the micro computer.